Letter

A high current gain gate-controlled lateral bipolar junction transistor with 90 nm CMOS technology for future RF SoC applications

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\textbf{A B S T R A C T}

A CMOS-compatible gate-controlled lateral BJT (GC-LBJT) was prepared with a conventional 90 nm CMOS technology for radio frequency system-on-chip (RF SoC) applications. The emitter injection efficiency and the doping profile in P-well were optimized by properly controlling source, drain, and well implants. Consequently, the GC-LBJT with a gate length of 0.15 \textmu m can achieve a current gain over 2000 and 17/19 GHz for the \textit{f\textsubscript{T}}/\textit{f\textsubscript{max}}, respectively, which are 1000\%, 200\%, and 60\% improvements in current gain, \textit{f\textsubscript{T}} and \textit{f\textsubscript{max}}, respectively as compared to the LBJT reported previously.

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1. Introduction

CMOSFET has been chosen preferably over bipolar junction transistor (BJT) in ULSI technology for its high integrability and relative low cost. However, for radio frequency (RF) applications, BJT is still superior to MOSFET for its well-behaved characteristics. Thus, many BJT based novel devices such as SiGe HBT, SiGe BiCMOS \cite{1–3}, and SOI lateral BJT \cite{8–10} have been developed. Nevertheless, these devices suffer also the drawback of complicated fabrication processes, and thus resulting in a high preparing cost. Recently, merging CMOS and BJT to form a lateral BJT (LBJT) has been studied extensively \cite{4–6} for RF SoC applications. The LBJT combines features of the high integrability and low cost in CMOS technology, and the well-behaved characteristics in BJT. In addition, the LBJT will be more powerful and applicable in coming nano CMOS technology regime for its ultra small lateral base width. However, these reported LBJT devices are just like a MOSFET operated in a lateral BJT mode. Even though the high integrability and the low cost have been kept, however, they have not been tuned to meet the requirements of RF applications.

In this work, we tuned the emitter/base and collector/base junctions' profile to develop a high performance gate-controlled lateral bipolar junction transistor (GC-LBJT) for future radio frequency applications. Besides, for a typical NPN LBJT, electrons from emitter inject both in lateral and vertical directions toward collector, and substrate, respectively, so that its performances are also seriously affected by the doping profile of the p-well (PW), i.e., the base region of the developed GC-LBJT. With an optimized tuning in these profiles, current gain (\textit{g}) over 2000, and cutoff frequency (\textit{f\textsubscript{T}}/\textit{f\textsubscript{max}}) equal to 17/19 GHz were achieved. It is worthy to note, not any mask was added to increase the preparing cost.

2. Experiments

The LBJT samples used for this study were prepared with a foundry’s 90-nm CMOS technology. The emitter-base(E/B) junction, collector–bases (C/B) junction, and well implant were tuned to optimize their profiles. In this work, we used three implant methods, i.e., standard, DSE (dedicated-sub-emitter), and dedicated-sub-collector (DSC) to tune these junctions into normal, sharp, and gradual junction profiles, respectively. In addition, three types of LBJT were split by the different implant methods and the various p-well (PW) doping. Fig. 1(a–c) shows the SUPREM-IV GS simulated cross-sections of the three types. In type 1 structure, owing to DSC and DSE implants, the profile of the regions near the collector side, and the emitter side are gradually, and sharp, respectively. Besides, the doping of PW implant for the base region is lower. In type 2 structure, only the DSC implant was applied in the region adjacent to collector for getting gradual C/B junction profile, but with a standard PW doping implant. This is same as the currently used NMOSFET, but operated in a lateral BJT mode.
In type 3 structure, both E/B and C/B junction profiles are sharp by the DSE implant, and has a lower doping PW. For comparison purpose, all types of NPN-LBJT sample were prepared with same emitter area, but split the gate length (i.e., base width) into 0.25 \( \mu \)m and 0.15 \( \mu \)m, respectively. The DC and RF properties were characterized with HP-4156 DC Parameter Analyzer, and HP-8510 Network Analyzer, respectively. Furthermore, Fig. 1(d) illustrates the top view of layout plan of the LBJT unit. The emitter E is enclosed by both collector C and base B to enhance emitter injection efficiency, and a 3 \times 3 LBJT array with the emitter unit area of 0.28 \( \mu \)m \times 0.4 \( \mu \)m is used to achieve 1 \( \mu \)m\(^2\) emitter area.

3. Results and discussion

Fig. 2 shows the DC current gain (\( \beta \)) as a function of collector current for various types and channel lengths NPN-LBJT samples. Because of the series resistances, and/or current crowding become significant under high current injection, all current gain decreases
with increasing collector current. Besides, the $\beta \sim (N_E/N_B) \times (1/W)$ [7], where $N_E$ and $N_B$ are impurity doping in emitter and base, respectively, and $W$ is base width, thus, the narrower base width will lead a shorter channel length to get a higher gain.

Among these types, the type 2 has the lowest $\beta$ due to the non-optimized E/B junction doping profiles (no DSE implant), which offers an extra emitter resistances $R_E$. In addition, the standard implant in the PW along the S/D gives a high impurity doping in base, thus lowering the $\beta$. In contrast, for the type 1, the DSE implant at emitter side reduces the $R_E$ and sharpens the E/B junction profile; consequently, the emitter efficiency $\gamma$. Besides, the DSC implant with less doping in collector shortens the base width, and the lower doping implant in PW lowers the base impurity concentration, thus achieving the highest current gain above 220, and 2000 for 0.25 $\mu$m, and 0.15 $\mu$m, respectively. Furthermore, in pre-

![Fig. 3. The Gummel plot and current gain (insert) for the type 1 NPN GC-LBJT with gate length of 0.25 $\mu$m, and emitter area of 1 $\mu$m$^2$ as a function of $V_{CE}$ with variations of $-0.12$ V to $-0.3$ V ($V_C = 0$ V, $V_B = 0$ V).](image1)

![Fig. 4. The output characteristics for the type 1 NPN GC-LBJT with gate length of 0.25 $\mu$m, and emitter area of 1 $\mu$m$^2$ as functions of $V_{CE}$ biased from 0 V to 1.2 V, and $V_{BE}$ biased from 0.78 V to 0.92 V ($V_{CE} = -0.3$ V, $V_E = 0$ V).](image2)

![Fig. 5. Normalized collectors current and drain current flicker noise vs. frequency. The 1/f flicker noise characteristic of the type 1 structure of the 0.25 $\mu$m NPN GC-LBJT with emitter area of 1 $\mu$m$^2$, and under bias condition of $V_{CE} = 0.65$ V, $V_{BE} = -0.3$ V, $V_{C} = 0$ V and the NMOSFET with gate area of 1 $\mu$m$^2$ under bias condition of $V_{GS} = 0.41$ V, $V_{DS} = 1.2$ V.](image3)
paring the type 3 structure, we used symmetric DSE implants at both E/B and C/B junctions, but kept lower PW implant to compare with the type 1 one. As shown in Fig. 2, $\beta$ of the type 3 is less than type 1, but higher than type 2 for both 0.25 $\mu$m, and 0.15 $\mu$m devices. This evidences the non-optimized E/B and C/B junction profiles, and well implant influence the current gain of LBJT significantly, especially for shorter channel length. For example, between type 2 and type 3, the difference in $\beta$ of 0.15 $\mu$m LBJT is larger than that for 0.25 $\mu$m, particularly under low current injection. Moreover, it has been reported [7], at low collector current; the $\gamma$ is dominated by the surface leakage rather than the useful diffusion current of minority across the base. Thus, for the type 2, the surface leakage is worsened by both non-optimized E/B junction profile and PW implant, and results in the lowest $\gamma$ and $\beta$. The shorter in channel length leads to the shallower in S/D junctions, thus getting the larger surface leakage to result in lower injection efficiency and current gain for the 0.15 $\mu$m samples. While, the very low current gain of the 0.15 $\mu$m type 2 sample in $I_c$ less than $10^{-6}$ A is suspected to the significant increase of NB after the PW implant in the shortened channel.

Fig. 3 presents the forward Gummel plot of the type 1 structure with gate length of 0.25 $\mu$m GC-LBJT under $V_{cb} = 0$, and $V_{be} = 0$ condition for various $V_{ce}$ and $V_{be}$, and its insert gives the $\beta$ vs. $I_c$ with $V_{ce}$ as a parameter, respectively. As shown, the $I_{off}$ currents of the GC-LBJT at $V_{be} = 0$ are very low $10^{-12}$–$10^{-14}$ A. In addition, following the increase of $V_{ce}$ from $-0.12$ V to $-0.3$ V, the $I_c$ currents are decreased for small $V_{be}$ (less than 0.5 V), but almost same for larger $V_{be}$. Besides, for all $V_{be}$, the changes in $I_b$ under different $V_{ce}$ are very small.

These phenomena imply under the low $V_{be}$, the hole accumulated in base caused by the high negative gate bias is higher than that the electrons injected from the emitter-base junction, consequently, the $\gamma$ and $I_c$ are main dependent on negative gate bias ($-V_{ce}$). However, under large $V_{be}$, the injection in E/B junction and thus both $I_c$ and $I_b$ become higher, in consequence, the effect of $V_{ce}$ is suppressed. Clearer results can be found from the insert, the current gains are plotted as a function of $I_b$ with $V_{ce}$ as parameter. As seen, under lower level injection, the current gain is higher for smaller negative $V_{ce}$ voltage, but it becomes saturated for large $V_{ce}$. Therefore, the gate bias plays an important role in operating the LBJT for various applications. Fig. 4 gives the output characteristics of the type 1 structure with gate length of 0.25 $\mu$m GC-LBJT under $V_{ce} = -0.3$ V, and $V_{be} = 0$ condition for various $V_{be}$ and $V_{ce}$. The plot reveals the high $\beta$ obviously.

Moreover, the 1/f noise is investigated, because it is an import issue in RF applications. Fig. 5 gives the normalized collector current 1/f flicker noise measured under different gate terminal bias as a function of frequency for the type 1 structure with gate length of 0.25 $\mu$m using 9812B Noise Prosystem, and compares it to a conventional NMOSFET with same emitter or gate area. To fairly compare, the 1/f noise level relative to the drive currents was used [11]. For the same emitter or gate area, GC-LBJT has lower noise level than that of NMOSFET by a factor over tenfold. However, we believe that the best comparison should be based on an application in circuit design.

<table>
<thead>
<tr>
<th>Lg</th>
<th>Bias</th>
<th>$V_g = -0.25$ V, $V_{ce} = 1$ V</th>
<th>$I_b = 3$mA</th>
<th>$V_g = 0.7$ V</th>
<th>$I_c = 80$ nA</th>
<th>$f_T$ (GHz)</th>
<th>$f_{max}$ (GHz)</th>
</tr>
</thead>
<tbody>
<tr>
<td>0.25</td>
<td>Type 1</td>
<td>250</td>
<td>13.37</td>
<td>2.45</td>
<td>5.44</td>
<td>8.5</td>
<td>13.3</td>
</tr>
<tr>
<td>0.25</td>
<td>Type 2</td>
<td>118</td>
<td>10.98</td>
<td>2.3</td>
<td>5.35</td>
<td>17.1</td>
<td>18.7</td>
</tr>
<tr>
<td>0.25</td>
<td>Type 3</td>
<td>220</td>
<td>6.84</td>
<td>1.7</td>
<td>5.35</td>
<td>17.1</td>
<td>18.7</td>
</tr>
<tr>
<td>0.15</td>
<td>Type 1</td>
<td>106</td>
<td>7.57</td>
<td>2.2</td>
<td>5.35</td>
<td>17.1</td>
<td>18.7</td>
</tr>
<tr>
<td>0.15</td>
<td>Type 2</td>
<td>281</td>
<td>7.57</td>
<td>2.15</td>
<td>5.84</td>
<td>11.2</td>
<td>16.1</td>
</tr>
</tbody>
</table>

Fig. 6. Comparison of (a) $f_T$ and (b) $f_{max}$ for type 1 to type 3 structures of the 0.25 $\mu$m and 0.15 $\mu$m NPN GC-LBJT with emitter area of 1 $\mu$m$^2$, and under condition of $V_{ce} = -0.3$ V, and $V_{be} = 0$ V, as a function of collector current.
where the design trade-offs and area and power consumptions can be compared to achieve certain performance specifications.

Furthermore, Table 1 lists the comparison of the \( \beta, V_a \) (early voltage), breakdown voltages \( V_{BCEO}, V_{BCEO}, f_T, \) and \( f_{max} \) among these three types of LBJT. The type 1 with gate length of 0.25 \( \mu \)m has the best performance of \( \beta, V_a, B_{CEO}, f_T, \) and \( f_{max} \) for real applications. It demonstrates also that the gradual profile of the DSC implant will lower electric field at collector sides.

Finally, the RF characteristics of the developed GC-LBJT are investigated with evaluation of the LBJT transistor’s S-parameters from 200 MHz to 50 GHz. Fig. 6 presents both \( f_T \) and \( f_{max} \) extracted form the measured H21 parameter and the unilateral power gain.

Both \( f_T \) and \( f_{max} \) increase with \( I_c \) firstly to a peak, then decrease for further increasing \( I_c \). For 0.25 \( \mu \)m LBJT with type 1 structure, the peak \( f_T \) and \( f_{max} \) are 8.3 and 13.5 GHz, respectively, but they even up to 17 and 19 GHz, respectively for a 0.15 \( \mu \)m one. Compared to the reported devices [5], the developed 0.15 \( \mu \)m LBJT has 1000%, 200%, and 60% improvements in \( \beta, f_T, \) and \( f_{max} \), respectively, where \( \tau \) is total delay time between emitter and collector, \( r_b \) and \( C_c \) are base resistance and collector capacitance, respectively. Therefore, the higher \( f_T \) and \( f_{max} \) for 0.15 \( \mu \)m type 1 LBJT is suspected from the contribution of the shorter base width, which is shorten also more by the gradual profile of the DSC implant in drain side and sharp profile of the DSE implant enhance emitter injection efficiency. Additionally, the larger difference in \( f_T \) between type 1 and type 3 for 0.15 \( \mu \)m devices than that for 0.25 \( \mu \)m devices can be explained with the same reasons. Thus, it is expected that the higher \( f_T \) and \( f_{max} \) could be achieved in the advanced nano CMOS technology.

4. Conclusion

A high performance CMOS-compatible gate-controlled lateral BJT has been successfully developed for RF SoC applications. Three structures with different channel length and various profile engineering including DSE, DSC and p-well implants were implemented by a 90 nm CMOS technology. Compared to the reported devices, the device with 0.15 \( \mu \)m channel length, gradual profile in the C/B junction, sharp profile in the E/B junction, and lower p-well implant for base region achieves 1000%, 200%, and 60% improvements in current gain, \( f_T \) and \( f_{max} \), respectively, thus is more preferable for future RF SoC applications.

Acknowledgments

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References