Stress-Induced Capacitance of Partially Depleted MOSFETs from Ring Oscillator Delay

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SUMMARY In the current study, stress-induced capacitance determined by direct measurement on MOSFETs was compared with that determined by indirect simulation through the delay of CMOS ring oscillators (ROs) fabricated side by side with MOSFETs. External compressive stresses were applied on \langle 110 \rangle silicon-on-insulator (SOI) n-/p-MOSFETs with the ROs in a longitudinal configuration. The measured gate capacitance decreased as the compressive stress on SOI increased, which agrees with the result of the capacitance difference between measured and simulated delay of the ROs. The oscillation frequency shift of the ROs should mainly be attributed to oxide capacitance, aside from the change in mobility of the n-/p-MOSFETs. The result suggests that the stress-induced gate capacitance of partially depleted MOSFETs is an important factor for the capacitance shift in a circuit and that ROs can be used in a vehicle to determine mechanical stress-induced gate capacitance in MOSFETs.

key words: Partially depleted MOSFET, strained channel, piezoresistance coefficient, ring oscillator, stress-induced capacitance

1. Introduction

Mechanical stress-induced effects on MOSFETs have been intensively studied to determine methods for increasing the speed of these devices [1]–[9]. Combined with silicon-on-insulator (SOI) technology, deep submicron strained MOSFETs enhance performance by lowering parasitic capacitance [10]. Previous measurements have enabled the evaluation of the mobility of \langle 110 \rangle SOI n-/p-MOSFETs under compressive stresses, i.e., piezoresistance coefficients. The coefficients not only depend on orientation, but also on strained configuration and SOI thickness [9]. Ring oscillators (ROs), which are fabricated with MOSFETs and composed of CMOSFETs, are commonly used as the benchmark of technology performance. ROs are generally used to evaluate the delay of logic gates resulting from any change in the fabrication process, such as the abovementioned process-induced mechanical stress. Studies have shown that both uniaxial and biaxial strain engineering can enhance or degrade n-/p-MOSFETs through induced stress to change effective electron or hole mass. However, only a few studies focused on the induced capacitance shift in integrated circuits, though induced depletion capacitance can affect the switching speed of logic gates. Suzuki et al. found that strain in the gate film changes the dielectric properties of MOSFETs [11]. Matsuda et al. fabricated n-MOSFETs with large gate areas to achieve a substantial change in gate capacitance [12]. However, direct measurement may become difficult for scaled-down devices because of the fringe effect. The current paper intends to explore stress-induced capacitance of MOSFETs through side-by-side RO delay and to compare the result with the direct measurement from MOSFETs under mechanical stresses. This approach may serve as an alternative method for evaluating stress-induced capacitance in scaled-down devices.

2. Experiment

Smart-cut silicon was used on an insulator wafer with a 200 nm-thick buried oxide. A 1.6 nm nitride gate oxide was grown and the 120 nm-thick poly-Si gate was attached. A 50 nm-thick nickel layer was deposited, followed by source/drain activation. Figure 1(a) illustrates the cross-sectional schematic of a MOSFET. A 70 nm contact etching stop layer (CESL) induced an initial compressive stress on the channel. The SOI thickness was 90 nm at the \langle 110 \rangle direction [13]. However, direct measurement may become difficult for scaled-down devices because of the fringe effect. The current paper intends to explore stress-induced capacitance of MOSFETs through side-by-side RO delay and to compare the result with the direct measurement from MOSFETs under mechanical stresses. This approach may serve as an alternative method for evaluating stress-induced capacitance in scaled-down devices.

Fig. 1 (a) Cross-sectional schematic of an SOI MOSFET, (b) schematic circuit of the measured RO, (c) the optical graph with MOSFETs and an RO, (d) rectangular cut of a wafer, allowing external stress longitudinal to the \langle 110 \rangle SOI channel of both MOSFETs and ROs, and (e) schematic of the compressive stress on both MOS and RO, where l is the distance from the clamping end to the location of the screw and Δd is the distance of the screw lift. The simulated arrows indicate the compressive/tensile stresses with magnification.
rection. The fully silicided (FUSI) metal gate approach was used because its work function can be adjusted through implantation doping. The CMOS ROs were fabricated with a gate channel width of 0.9 and 0.45 \( \mu \)m for the pMOSFETs and nMOSFETs, respectively, and a channel length of 0.09 \( \mu \)m. Figure 1(b) shows the schematic of an RO with 53 stage inverters and 64 optional capacitive loadings from a minimum of 0 fF (no loading) to 2 pF. The current study selected no capacitive loading to allocate delay time on CMOSFETs. The optical graph shows a typical distance, approximately 1200 \( \mu \)m, between MOSFETs and an RO [Fig. 1(c)]. The contact pads were connected through the manipulation of probes using HP4156 semiconductor parameters and with an HP-4284A LCR Analyzer for the capacitance-voltage (C-V) plot. The wafer containing n-/p-channel MOSFETs and ROs was cut to approximately 1 cm \( \times \) 4 cm [Fig. 1(d)], the dimension of which is comparably larger than the distance between the MOSFETs and the RO shown in Fig. 1(c). The rectangular cut allowed external stress to be applied onto the \( \langle 110 \rangle \) SOI channel. The external stress measurement setup is comprised of a customized apparatus that allows a cut silicon bar to be clamped onto one side. A loading force on the other free end creates a uniaxial longitudinal stress onto the channels. On the cross-section, the top surface is placed under the highest compressive stress, whereas the counterpart bottom surface is placed under the highest tensile stress [Fig. 1(e)], in which the arrows show that the upper portion of the silicon bar bears compressive stresses (inward arrows) while the lower portion bears tensile stresses (outward arrows). Lift distance (\( \Delta d \)) was measured based on the number of turns a delicate screw makes through a hole underneath. Given that the distance from the measuring device to the screw end (\( l \)) was kept constant, the stress on the channel was obtained by multiplying the Young’s modulus of silicon (150 GPa) by the strain (\( \Delta l/l \)) of the silicon bar. The stresses were 5.1, 20.3, and 45.7 MPa for the screw lifts at 1/4, 2/4, and 3/4 turns, respectively. Oscillation frequencies of the ROs were measured using an 8563EC spectrum analyzer and a DSO8104A oscilloscope.

3. Results and Discussion

3.1 MOSFET Characterization

Figures 2(a) and (b) demonstrate the drain current of n-/p-MOSFETs under stresses. The measured current change shifted under external mechanical stresses because of effective mass change. Table 1 lists the normalized saturation current changes with external stresses from 5.1 MPa to 45.7 MPa for pMOSFET and nMOSFET, respectively. For compressive stress, the piezoresistance coefficient is negative for the n-type, whereas the p-type is positive for the \( \langle 110 \rangle \) silicon. Given that the Young’s modulus of silicon is approximately 185 GPa, the deformation under 45.7 MPa is approximately 0.02%. Thus, the dimensional deformation of a channel is negligible in this case. The saturation current is proportional to the carrier mobility for both n-/p-MOSFETs. Additionally, the reciprocal ratio of (\( \Delta I_D/I_D \)) on stress change (\( \Delta \sigma \)) is approximately the same as the piezoresistance coefficients when the \( \Delta I_D \) is relatively small, which has been previously discussed [9]. That is,

\[
\frac{\Delta I_D}{I_D} \approx \frac{\Delta \mu}{\mu} = \pi \cdot \Delta \sigma
\]

where \( \pi \) is the piezoresistance coefficient of \( \langle 110 \rangle \) channel in this case under longitudinal configuration, and \( \Delta \sigma \) is the stress variation.

Figure 3 shows that the threshold voltage (\( V_T \)) changes under stresses. The \( V_T \) changes are somewhat insignificant.
Fig. 3  $V_t$ changes of the n-/p-MOSFET under stress.

under 45.7 MPa. Nevertheless, $V_t$ is correlated with external stress because it is a function of the intrinsic Fermi level ($E_i - E_F$) [13]. Figures 4(a) and (b) demonstrate capacitance versus gate voltage under stresses for nMOSFET and pMOSFET, respectively, in which the capacitance decreases with increasing stress. Figure 4(c) summarizes the normalized gate capacitance ($\Delta C/C$) from Figs. 4(a) and 4(b). The decreasing capacitance with applied compressive stress concurs with previously reported findings [12]. Given that the shifts mostly occur at the weak inversion region rather than at the accumulation region, these capacitance shifts may be mostly attributed to depletion charge. These phenomena imply that mechanical stress-induced effects should alter depletion charges, probably resulting from the strained channel because of increasing stress.

3.2 Oscillation Frequency Simulation and Measurements of ROs

The oscillation frequency of the ROs was simulated using the advanced design system developed by Agilent. The $\mu_n$ and $\mu_p$ in the BSIM3 model were adjusted in accordance with the measured mobility change under 45.7 MPa to represent the stress. These modified electron and hole mobilities were applied to evaluate the oscillation frequencies of the ROs. Figure 5 shows the normalized frequencies that yielded to compressive stresses perpendicular to the channel (longitudinal configuration) under measurement and simulation using the modified mobilities of the RO with 5.1, 20.3, and 45.7 MPa. The open and solid marks indicate the simulated and experimental ratios, respectively. The simulation ratio increases to 1.74%, whereas the experimental ratio increases to 1.32% at 45.7 MPa. The overestimated ratio in the simulated result implies a number of other factors aside from mobility changes. This phenomenon could be attributed to gate oxide capacitance shifting because this trend agrees with what is found in Fig. 4(c). Although a standard MOSFET may amount to over a few percentage points because of the variability in transistor characteristics, the variation may be low because the chosen devices are fabricated side by side. By subtracting the shifting mobility factor from the measured delay, the shifting capacitance in the ROs when external stresses are applied may be approximated.

3.3 Induced Capacitance in ROs

The RO comprises the n-stage CMOS inverters. The frequency ($f$) set by power consumption and capacitance at
each node is as follows [14]:

\[
f = \frac{1}{2nTD} \approx \frac{\mu_{eff} \cdot W_{eff} \cdot C_{ox} \cdot \Delta V^2}{8 \cdot \eta \cdot n \cdot L \cdot q_{max}},
\]

\[
W_{eff} = W_n + W_p,
\]

\[
\mu_{eff} = \frac{\mu_n \cdot W_n + \mu_p \cdot W_p}{W_n + W_p},
\]

where \( n \) is the number of stages, \( T_D \) is the delay time of a single stage, \( C_{ox} \) is the oxide capacitance, \( \Delta V \) denotes the gate overdrive in the middle of transition, \( q_{max} \) is the maximum charge in the output node, \( \eta \) represents a constant, \( W_n \) and \( W_p \) are the channel widths of nMOSFET and pMOSFET, respectively, and \( L \) is the channel length. Assuming \( W_p = \alpha W_n (\alpha=2 \text{ in this case}) \), the overdrive voltage (\( \Delta V \)) is rather small compared with the mobility change (piezoresistance effect) because the maximum \( V_i \) variation under 45.7 MPa is approximately 0.4% with a 0.02% deformation, which is relatively low dependent on mechanical stress even up to 100 MPa in a previous report [15]. For a partially depleted MOSFET, the total oxide capacitance (\( C_{total} \)) is determined by the depletion layer width in addition to intrinsic oxide, that is,

\[
\frac{1}{C_{total}} = \frac{1}{C_{ox}} + \frac{1}{C_{dep}} = \frac{1}{C_{ox}} + \frac{1}{C_{dep}} + \frac{1}{\varepsilon_S},
\]

where \( C_{ox} \) is the oxide capacitance dominated by insulator properties, \( C_{dep} \) denotes the depletion-layer capacitance in the inversion region, \( \varepsilon_S \) represents the silicon permittivity, and \( W \) is the width of the depletion layer. The maximum width of depletion layer \( W \) depends only on the intrinsic Fermi level (\( E_F \)).

Oxide capacitance and carrier mobility are dominant factors in the oscillation frequency shift with mechanical stress. Thus, the evaluation of the oscillation frequency shift of an RO can depend on the normalized oscillation frequency, which is simplified by the following partial derivative equation:

\[
\frac{\partial f}{f} = \frac{\partial M(\mu_n, \mu_p)}{M(\mu_n, \mu_p)} + \frac{\partial C}{C},
\]

Table 2 summarizes the experimental/simulated normalized frequency, mobility, and capacitance of an RO. Results showed that the compressive stress can boost the speed of the RO, but also eliminate the speed due to reduced capacitance. The higher the stress on the RO, the higher the speed of the RO. The indirect calculated \( \Delta C/C \) from the experimental results seems to have a better approximation near the measurement result than the simulated one. The induced layout effect could be the factor that decreases the capacitance shift under stresses, but this effect may be difficult to predict.

4. Conclusions

Mechanical stress-induced effect is an important issue in the scaling down of semiconductor devices. Direct measurements of capacitance change may require large area capacitance. The current study successfully demonstrates that the side-by-side fabricated transistors and ROs provide an alternative approach to evaluate the induced depletion-layer capacitance of a circuit under compressive stress. On the other hand, tensile stress can enhance the mobilities of both n-/p-MOSFET [4], [7], [15]–[17] under (110) transverse configuration. The result is expected to promote the speed of an RO consisting of n-/p-MOSFET. The capacitance is also found to increase rather than decrease under tensile stress [12]. The tendency of both mobility and capacitance should boost the speed of an RO. The reduced capacitance expected via simulation and experiment is likely consistent with the result by direct C-V measurement. Additionally, partially depleted MOSFETs may be only suitable in this application because
the capacitance is stress induced.

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References